

A method comprising:

receiving a request from a first computer system for identification of a second computer system;

retrieving an identifier that identifies the second computer system;

encrypting the identifier with a key associated with the first computer system to produce a hash value; and

providing the hash value to the first computer system in response to the request.

The method of claim 1, wherein the act of retrieving the identifier 2. comprises:

retrieving a processor number that identifies a processor of the second computer system.

- The method of claim 2, further comprising: 3. executing a processor instruction; and retrieving the number in response to the execution of the instruction.
- The method of claim 1, further comprising: 4. receiving the key from the first computer system.
- 5. The method of claim 1, wherein the key indicates an address of a web site.

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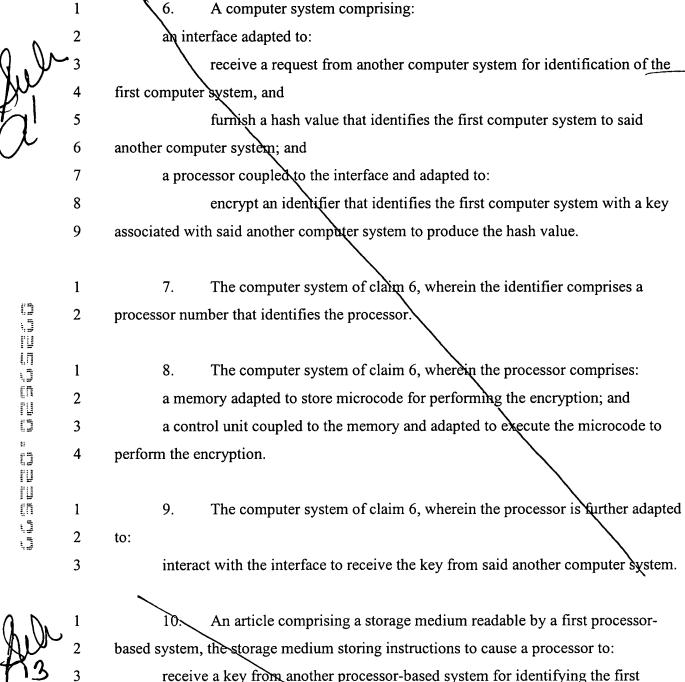
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determine whether the key is valid,

identifies the first system with the key to produce a hash value.

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6 7 system,

based on the identification, selectively authorize encryption of an identifier that

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1 11. The article of claim 10, the storage medium storing instructions to cause 2 the processor to:
3 use an address of said another system to determine whether the key is valid.
1 12. The article of claim 11, wherein the key indicates an URL address.
1 13. The article of claim 10, the storage medium storing instructions to cause

the processor to:

execute an instruction to cause the processor to subsequently use the key to produce the hash value.

14. The article of claim 10, wherein the identifier comprises a processor number.

## 15. A microprocessor comprising:

an instruction unit adapted to indicate when the instruction unit receives an instruction that requests an identifier that identifies the microprocessor;

an execution unit coupled to the instruction unit and adapted to, in response to the indication from the instruction unit, encrypt a key with the identifier to produce a hash value; and

a bus interface unit coupled to the execution unit and adapted to furnish an indication of the hash value to external pins of the microprocessor.

The microprocessor of claim 15, wherein the execution unit comprises:

a control unit coupled to the algorithmic unit and the registers; and

a memory coupled to the control unit and storing microcode to cause the control
unit to use the key and the identifier to produce the hash value.



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17. The microprocessor of claim 15, wherein the identifier comprises a processor number.

- 18. The microprocessor of claim 15, wherein the execution unit is adapted to use a one way hash function to produce the hash value.
- 19. The microprocessor claim 15, wherein the execution unit is adapted to use a non-commutative hash function to produce the hash value.
- 20. The microprocessor of claim 15, wherein the execution unit is adapted to use a collision free hash function to produce the hash value.